SOFTWARE DEFINED RADIO

SPEAKEASY PHASE -II

M. PREETHIKA

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SPEAK EASY PHASE II

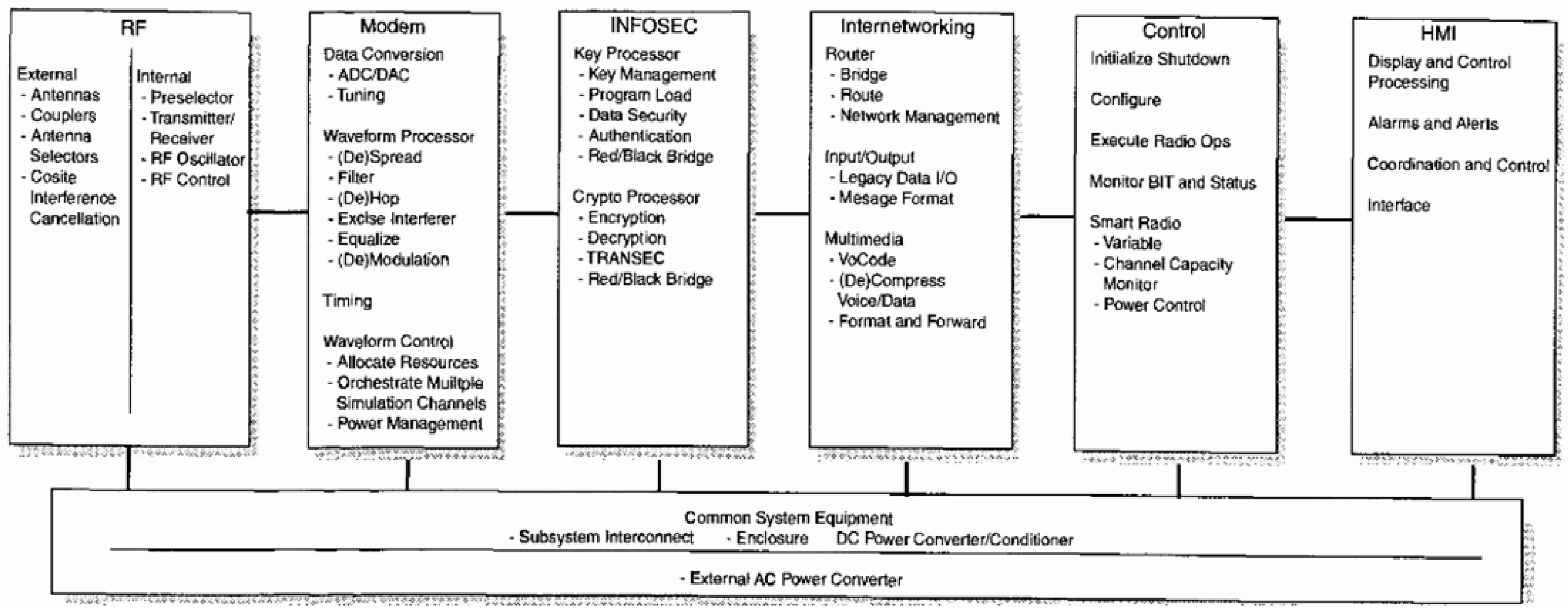
The Second Phase of the speakeasy project was contracted to Motorola, IIT, and Sanders. Its four year program sought to design successively more refined software radios and to formalize an architecture. Instead of emphasizing just the MCM and CYPRIS aspects of the radio, Phase II's focus was the entire radio. Phase II also paid more attention to the software raspects of the radio than phase I, important philosophically to building a software radio. The phase II architecture also formed a more structured solution to incorporating both secure (black) and unsecure (red) modules into a single architecture.

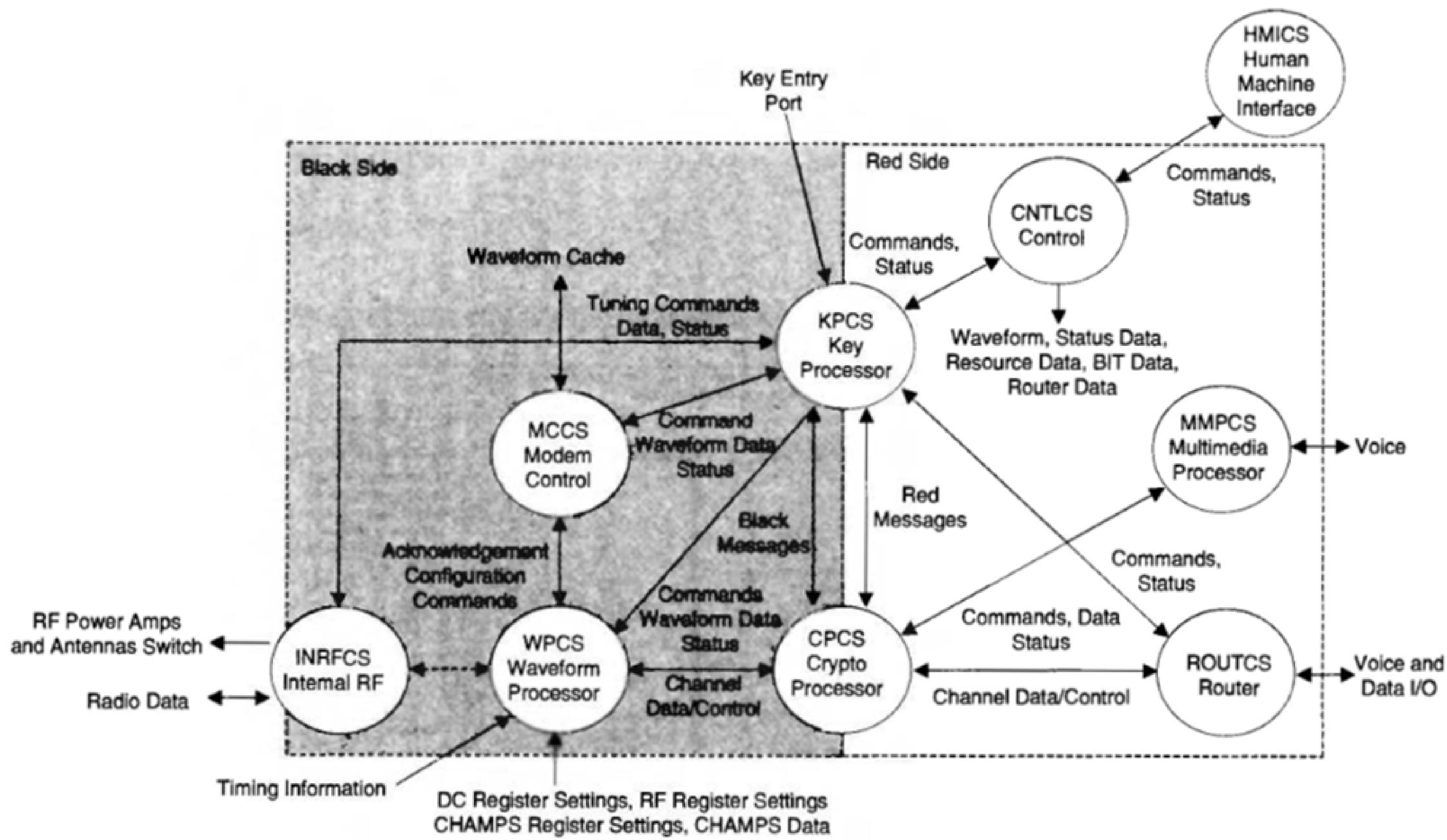
The primary goals of phase II architecture were to

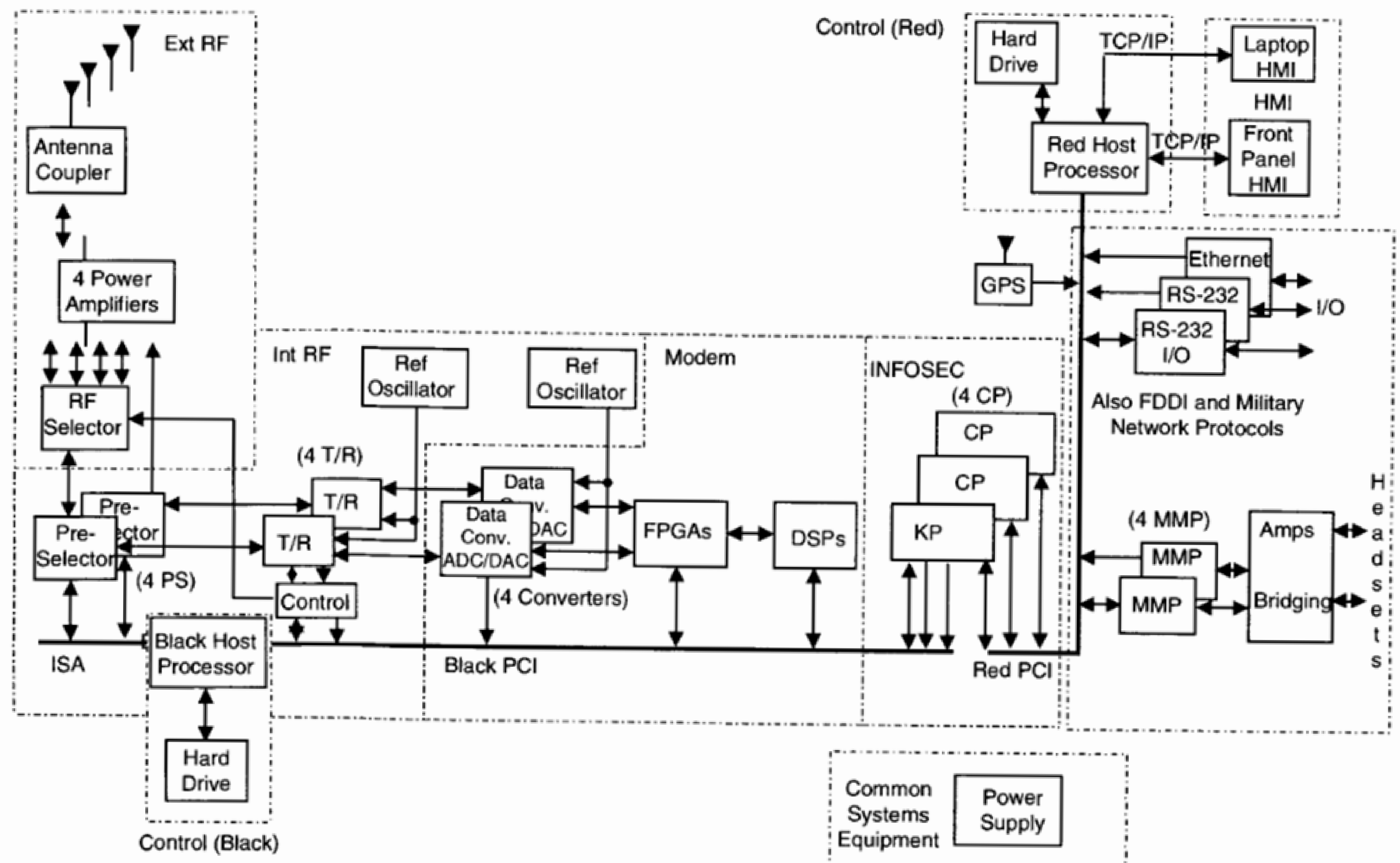
→ Implement a reconfigurable architecture,

→ Implement an open architecture.

→ achieve cross channel connectivity


RF
External
- Antennas
- Couplers
- Antenna Selectors
- Cosite Interference Cancellation
Internal
- Preselector
- Transmitter/ Receiver
- RF Oscillator
- RF Control
Modem
Data Conversion
- ADC/DAC
- Tuning
Waveform Processor
- (De)Spread
- Filter
- (De)Hop
- Exclse Interferer
- Equalize
- (De)Modulation
Timing
Waveform Control
- Allocate Resources
- Orchestrate Muiltple Simulation Channels
- Power Management
INFOSEC
Key Processor
- Key Management
- Program Load
- Data Security
- Authentication
- Red/Black Bridge
Crypto Processor
- Encryption
- Decryption
- TRANSEC
- Red/Black Bridge
Internetworking
Router
- Bridge
- Route
- Network Management
Input/Output
- Legacy Data I/O
- Mesage Format
Multimedia
- VoCode
- (De)Compress Voice/Data
- Format and Forward
Control
Initialize Shutdown
Configure
Execute Radio Ops
Monitor BIT and Status
Smart Radio
- Variable
- Channel Capacity Monitor
- Power Control
HMI
Display and Control Processing
Alarms and Alerts
Coordination and Control
Interface
Common System Equipment
- Subsystem Interconnect
- Enclosure
DC Power Converter/Conditioner
- External AC Power Converter


Key Entry Port
Black Side
Red Side
HMICS Human Machine Interface
Commands, Status
CNTLCS Control
Commands, Status
Waveform Cache
Tuning Commands Data, Status
KPCS Key Processor
Waveform, Status Data, Resource Data, BIT Data, Router Data
MCCS Modem Control
Command Waveform Data Status
MMPCS Multimedia Processor
Voice
Red Messages
Black Messages
Acknowledgement Configuration Commands
Commands, Status
Commands Waveform Data Status
Commands, Data Status
RF Power Amps and Antennas Switch
INRFCS Internal RF
WPCS Waveform Processor
CPCS Crypto Processor
ROUTCS Router
Voice and Data I/O
Radio Data
Channel Data/Control
Channel Data/Control
Timing Information
DC Register Settings, RF Register Settings
CHAMPS Register Settings, CHAMPS Data



Ext RF
Antenna Coupler
4 Power Amplifiers
RF Selector
Pre-Selector
Pre-Selector
(4 PS)
ISA
Black Host Processor
Hard Drive
Control (Black)
Int RF
(4 T/R)
T/R
T/R
Control
Ref Oscillator
Ref Oscillator
Data Conv. ADC/DAC
(4 Converters)
Black PCI
Modem
FPGAs
DSPs
INFOSEC
(4 CP)
CP
CP
KP
Red PCI
Control (Red)
Hard Drive
Red Host Processor
TCP/IP
TCP/IP
Laptop HMI
HMI
Front Panel HMI
GPS
Ethernet
RS-232
RS-232 I/O
I/O
Also FDDI and Military Network Protocols
(4 MMP)
MMP
MMP
Amps
Bridging
Headsets
Common Systems Equipment
Power Supply

Secondary goals to

→ incorporate more commercial off-the-shelf (COTS) components.

→ reduce the form factor to a size deployable in the field,

→ incorporate reconfigurable hardware,

→ Improve the CYPRIS Chip's context-switching time

PHASE II ARCHITECTURE

The system-level modules support various functions

→ The RF module supports four half-duplex Channels, ideally operating from 2 MHz to 2 GHz and is divided into internal and external Components.

→ The modem module performs data conversion, waveform processing over four independent Channels, and resource allocation.

→ The INFOSEC module contains both key and Crypto processors, which are not strictly limited to be placed on the same chip as was done on Cypris.

→ The interworking module provides cross-Channel connectivity and I/O capabilities.

→ The control module monitors the radio and performs system-level control operations. It allows certain operations, such as power control, to be controlled independently by the radio. Functions that the radio can independently set and control in response to environmental changes are termed smart radio functions.

→ The HMI module provides an interface for displaying the status of the radio as well as providing a control interface.

The funtional flow model of Phase I naturally leads to a procedural approach, particularly in software. While procedural implementations are useful for implementing individual algorithms, their lack of modularity typically leads to a complete redesign, if only of the software, to support new functions, almost defeating the purpose of a software radio.

→ The module-defined basis of the Phase II architecture naturally leands itsely. to a modular architecture and typically a more object-oriented software structure. A software architecture based on object-oriented methodologies ~~leads~~ is quite powerful since it tends to result in a "more modular" and more flexible software architecture and, in turn, a more flexible overall architecture.

Fig 2

Each software module used in Phase II's architecture performs a specific function :

→ Internal RF control Software (INRFCS) sends the various control messages required to the RF components,

→ Modem Control Computer Software (MCCS) performs resource allocation tasks,

→ Waveform Processing Computer Softwar (WPCS) performs the waveform - specific processing tasks, such as modulation, despreading and interleaving.

→ key processing Computer Software (KPCS) and cryptographic Processor Computer Software (CPCS) jointly performs the radio's INFOSEC functions,

→ Multimedia Processing Computer Software (MMPCS) performs vocoder tasks and bridging between the voice Channels.

→ Control Computer software (CNTLCS) performs the system's control operations, such as startup, channel setup and monitoring system status.

→ Routing Computer software (ROUTCS) supplies the system's networking capabilities

→ Human Machine Interface Computer Software (HMICS) supplies a local or remote operator control of the system.

Various functions needed to implement the radio were encapsulated into well-defined and distinct modules. Each module could then be implemented or altered fairly independently as logng as the module provides the interfaces and services it is specified to contain.

⇒ Communication between the modules occurs without the use of a centralized operating system; instead, the modules simultaneously pass multiple asynchronous messages over the system's peripheral component interconnect (PCI) bus.

⇒ The three software layers used are .

* the link layer, which performs the data transfers over a hardware bus;

* the communications layer, which creates and services virtual channels between agents; and

* the application layer, which houses the modules pictured in figure.

(The PCI bus forms a fourth layer as the physical layer.)

⇒ Similar to the software modules' encapsulation, the layers' tasks are isolated from eachother.

The interfaces between these layers are defined through a predetermined set of functions. Messages are constructed using these three layers and their interface functions.

⇒ The use of layers and standardized interfaces help to obstract the functions of the radio, to provide an isolation of tasks, and to move the architecture toward a more open design. This simplifies the replacement of individual software modules, thus improving reconfigurabdity since each module does not need knowledge of the internal operations of the other modules, only their functionality and their interfaces.

SPEAK easy Phase II's hardware architecture, which used COTS components for 70% of its devices, clearly defines and separates the red and black processing elements and supports four channels over its PCI and Instruction Set Architecture (ISA) buses.

→ Information flow between the red and the black architecture is managed by the INFOSEC device, which has four cryptographic processors (CP) and one key Processor (KP).

→ Data Conversion between the analog and digital domains is performed by the data Converter modules.

→ Analog translation between IF and baseband is performed by transmit/Receive (T/R) units.

→ The RF capabilities were again defined to range from 2MHz to 2GHz with this functionality supported through switching.

→ Multichassis Multilink Point to point protocol (MMP) devices provide the connections to voice lines, which may also be bridged together.

→ Standard civilian and military network connections are also provided.

→ Baseband processing is performed in DSPs (Texas Instruments' C44s) and FPGAs (CHAMPS- configurable Hardware Algorithm - Mappable Processors).

→ Wireline connectivity is provided for a suite of serial and network protocols including RS-232, Etherenet and Ethernet, fiber Distributed Data Interface (FDDI).

The inclusion of FPGAs in Phase II's architecture is an important concept for Software radios.

⇒ In addition to an FPGA's performance advantages for algorithms that have deep pipelines or can be split into parallel branches, the inclusion of FPGAs also enables the phase II architecture to reconfigure its software and its hardware.

Utilization of reconfigurable hardware gives a software radio architecture the ability to somewhat tailor its resources to the current application, giving the architecture added flexibility and potentially increased processing efficiency.

⇒ However some of the additional design challenges when using reconfigurable hardware in a software radio design are not seen when using standard processors. The most critical of these challenges is the time required to reprogram reconfigurable hardware.

→ To ~~reconfi~~ reprogram reconfigurable hardwarde, the entire chip typically needs to be reprogrammed, a program that may take several milliseconds and which is difficult, if not impossible, to accommodate if the reconfigurable hardware is used in real-time stream.

→ In fact CYPRIS had to be removed from Phase II because of its excessively long context-switching times and replaced with a new INFOSEC Chip developed under phase II, the advanced INFOSEC Machine (AIM) chip.

⇒ The AIM Chip operates at 100 MHz and utilizes three RISC processors and an array of specialized cryptographic components. Two of the processors perform crypto processing, and the other performs key processing.

It can provide multiple simultaneous levels of security across four independent channels - important for a multichannel software radio employing INFOSEC.

It also allows for single clock cycle switching between algorithms aided by the use of shadow registers to preload the next algorithm, solving the context - switching problems of CYPRIS.