Software Defined Radio -

Speakeasy Phase - I

Architecture

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Speakeasy:

* Speakeasy was one of the software radio Architecture and a joint Project of the branches of the US military.

* Initially, Research was originated as part of the Air force's Tactical AntiJam programmable signal Processor (TAJPSP), which sought to create a programmable modem that would support the future evolution of waveforms.

* During operation Desert Storm, other military branches observed that their operation were being hindered by radios, that were not interoperable with allies radios.

* Other military branches took an interest in TAJPSP, and the collective efforts of all branches developed into SPEAKEASY program.

* This new program expanded the original goals of TAJPSP to the creation of software defined MBMMR.

* Speakeasy was the beginning of a long term strategy by military to advance software radio Technology. and to decrease costs by leveraging the commercial mass market.

* Then, the military planned to develop and implement a software radio architecture with commercial partners and then to later support the migration of technology to commercial domain.

* Speakeasy program was broken into 2 phases,

* Speakeasy phase 1
* Speakeasy phase 2

* Phase 1 works to demonstrate the feasibility of software radio and the suitability of software radio for acting as MBMMRs with special attention paid to creating software reconfigurable antenna.

* Phase 2 sought to create a viable implementation of software radio and to formalize a complete software radio Architecture.

Speakeasy phase 1 :

* Phase 1 (1992 to 1995), was primarily contracted to Hazeltine, TRW, Lockheed - Martin, Motorola and Rockwell collins.

* It was intended to show that software radio had the potential to,

* Alleviate the military's interoperability issues.

* Simplify the process of incorporating new technology.

* Provide more advanced security function.

* Simplify information security (INFOSEC) implementations.

* Add flexibility without significantly increasing power consumption.

* Demonstrate that the use of reprogrammable hardware in the place of dedicated hardware would incur no major performance penalties.

* Phase 1 utilized two concepts,

(i) multibanding through selectable subbands implemented with multiple RF front ends.

(ii) And accomplishing INFOSEC functions in programmable device.

Architecture :

* The architecture implements a four channel half duplex transceiver with the bulk of processing being performed in DSP.

* The various hardware components are housed inside a Versa module Europa (VME) chassis.

* The VME bus transports commands and control functions as well as low data rate signals.

* The architecture supports reconfiguration through reprogramming the quad c40 subsystem and INFOSEC subsystem.

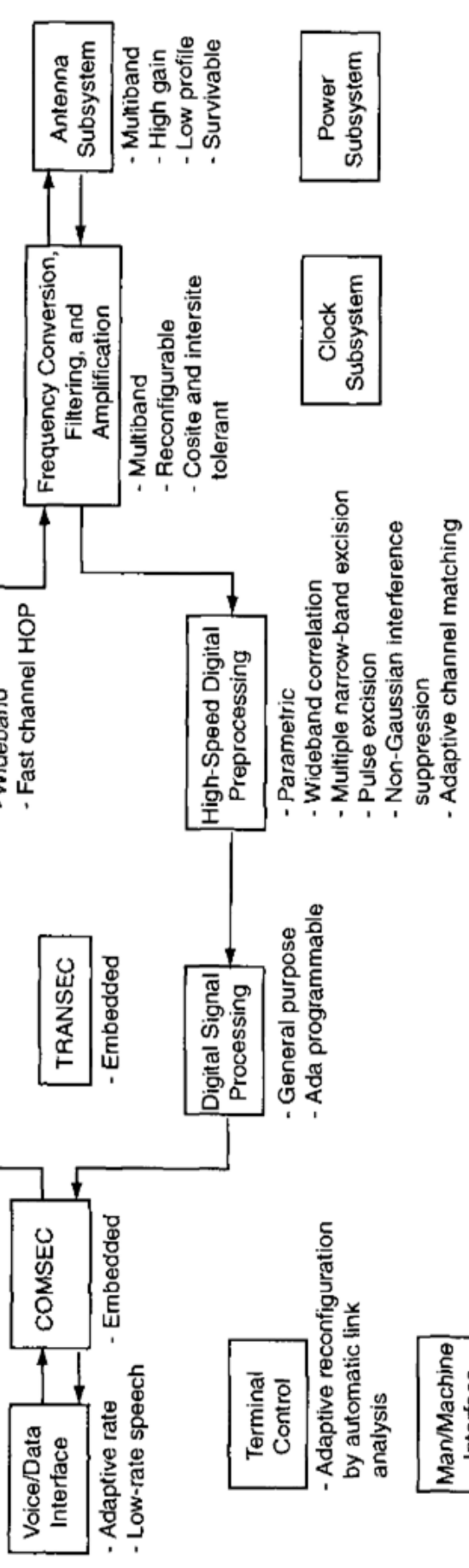* To handle high data rate signals, a segmented, a high speed bus is implemented on the backbone of the chassis.

* Control and monitoring of the radio is performed from a sun SPARC workstation.

* To provide multiband capability, the radio was defined to operate from 2 MHz to 2 GHz.

* To maintain performance & linearity, the frequency range was segmented into 3 bands.

Overall Features
- Multiple simultaneous waveforms
- Modular open architecture
- Common module emphasis
- Integrated diagnostics
- Graceful degradation, self-reconfigurable

Antenna Subsystem
- Multiband
- High gain
- Low profile
- Survivable

Power Subsystem

Clock Subsystem

Frequency Conversion, Filtering, and Amplification
- Multiband
- Reconfigurable
- Cosite and intersite tolerant

Waveform Synthesis
- Parametric
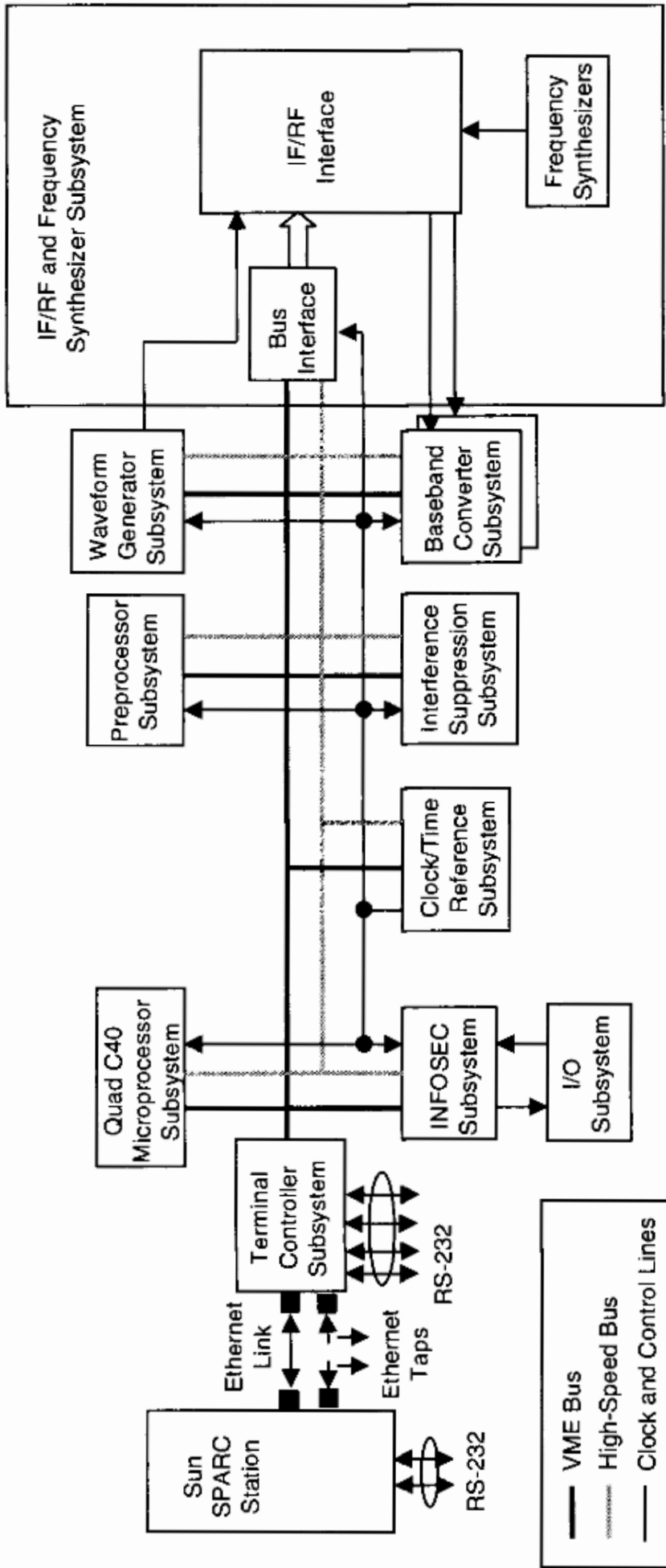- Wideband
- Fast channel HOP

High-Speed Digital Preprocessing
- Parametric
- Wideband correlation
- Multiple narrow-band excision
- Pulse excision
- Non-Gaussian interference suppression
- Adaptive channel matching

TRANSEC
- Embedded

Digital Signal Processing
- General purpose
- Ada programmable

COMSEC
- Embedded

Voice/Data Interface
- Adaptive rate
- Low-rate speech

Terminal Control
- Adaptive reconfiguration by automatic link analysis

Man/Machine Interface
- Single training, logistics, and maintenance process
- Minimized operator involvement

IF/RF and Frequency Synthesizer Subsystem

IF/RF Interface

Frequency Synthesizers

Bus Interface

Waveform Generator Subsystem

Baseband Converter Subsystem

Preprocessor Subsystem

Interference Suppression Subsystem

Clock/Time Reference Subsystem

Quad C40 Microprocessor Subsystem

INFOSEC Subsystem

I/O Subsystem

Terminal Controller Subsystem

Ethernet Link

Ethernet Taps

RS-232

Sun SPARC Station

RS-232

VME Bus
High-Speed Bus
Clock and Control Lines

(i) a low band from 2 MHz to 30 MHz

(ii) a mid band from 30 MHz to 400 MHz

(iii) a high band from 400 MHz to 2 GHz

* These 3 bands were then implemented as independent RF channel with components designed to support the band specific to that channel.

* Multichip Module (MCM) was designed to provide processing power for modem.

* MCM consists of 4 Texas instruments C40s, a PLD and 5 MB of memory, of which 1MB acts as a shared global memory for 4 processors.

* Each of the 4 DSPs handles an individual radio signal.

* The PLD handles bus arbitration and interrupt handling.

* The implementation of MCM showed that 1995 technology could use reprogrammable components, non just dedicated hardware, to achieve high performance using less than 10 watts of power and three inch square form factor to implement real world waveforms.

* The development of cryptographic Reduced instruction set (CYPRIS) chip was another key result of phase 1.

* Previously, each military radio had a dedicated chip for unique INFOSEC function.

* To solve these issues, a processing solution capable of implementing a wide variety of INFOSEC function was needed.

* Since speakeasy is a multichannel system, several different security algorithm may need to be run simultaneously and independently.

* To provide the required raw computational power with an appropriate level of security, new chip - CYPRIS. was developed.

* The CYPRIS chip allows for the implementation of INFOSEC function on its RISC (Reduced instruction set computer) processor and its reconfigurable hardware.

* Since it is programmable, the CYPRIS chip can support a wide range of INFOSEC protocols by implementing the new.

algorithm on Risc chip , on the reconfigurable fabric , or access both , depending upon the combination that results in most efficient implementation .

   * Although developed in phase I, CYPRIS was not used until phase II

Diagram :

(i) Refer Speakeasy phase -1 Data flow.

   fig 9.2 - 453

(ii) Refer Speakeasy phase - 1 Architecture

   fig 9.3 - 454 .